IA32: from Intel or AMD?

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Abstract.

With the new Pentium 4 architecture, Intel tried to improve the performance of his processors. The fact is, Pentium 4 is a new generation of processors and not an evolution of Pentium III processor architecture or other Pentium architectures.[1] In Pentium 4, the pipelines were increased and it as also a bigger target buffer that the existing in Pentium III, while AMD processors have low energy consumption and produces less heat.

The overheating of Intel Prescott processor and his high energy consumption make it slower than Northwood, while AMD processors still have better performances, what made Intel go back and re-adapt Pentium III when for use in notebook computers.

AMD Athlon processors, using 12 stages against 20 on Pentium 4 generation, and including an I/O Hypertransport system in the processor core, were faster than the first generation of Pentium 4, which have a great dependence on the rest of the machine. On the other side, AMD rates his processor using "PR" scale for his processor, what made them lost the "marketing campaign" for Intel, often their processors were faster.

1 Introduction

Central Process Unit (CPU), or simply "processor", is the main component in a computer, that interprets instructions and processes data. Along time, processors give way to many developments and become mass produced, suited for many purposes.

The standardization begins from transistor mainframes and rapidly acclerated until today, specially due to popularization of integrated circuits (IC´s). This circuits allows CPUs to be designed in very small areas, on the order of millimetres, and this made microprocessors, and particularly CPUs, appear in almost everything, since mobile phones until automobiles.

2 Features

Intel Pentium III[2]

Pentium III processor processor have 3 diferent generations along his life: *Katmai*, *Coppermine* and *Tualatin*. The first version of Pentium III, *Katmai*, was very similar to Pentium II, using an L1 cache for instructions and data ("Harvard" architecture).

Pentium III maintains compatibility with Pentium II but have new improvements, such as:

- Nem 70 SSE (*Streaming SIMD Extensions)* instructions - named *Katmai* - for better perfomances with 3D graphics, video, audio and internet;
- 12 new instructions as complement of the 57 MMX instructions used in Pentium II;
- 8 new instructions to control L1 cache with 32 kB, what results in a better performance of processor;

Contrary to Pentium III, this new SSE instructions made now possible the use of floating point and integer unit, while Pentium II only allows have integer unit. Also includes DIB [1] architecture (already present in Pentium II) and 10 stages of pipeline.

On October, 1999, the second version of Pentium III, named Coppermine, was released and offers a low latency cache L2, with 256 kB and full-speed (works with same frequency as the processor). This have a new cache system, named *Advanced Transfer Cache (ATC)*, which improves the bandwidth between L2 cache and core of processor. Some lacks of pipeline were also solved and Coppermine works 30% faster than the earlier version, but it can´t go faster than 1,13 GHz, due to some heat problems and Pentium III allows symmetric processing (more than 1 processor on board).

Tualatin was the third version of Pentium III, but it was more an experiment for Pentium 4 due to its 0,13 µm size and its 512 kB L2 cache on-chip. Resuming:

	Pentium III Katmai	**Pentium III Coppermine**	**Pentium III Tualatin**
Release date	February, 1999	October, 1999	July, 2001
Improvements	- 0,25 µm; - 70 new SSE instructions; - FSB 100 or 133 MHz; - 32 kB L1 cache on chip; - 512 kB L2 cache off chip.	- 0,18 µm; - 32 kB L1 cache on chip; - 256 kB L2 cache on chip ATC;	- 0,13 µm; - 512 kB L2 cache on chip ATC.

Table 1 – Generic specifications of Pentium III family

Intel Pentium III competes with AMD K6-III, AMD Athlon K7, AMD Athlon K75 and AMD Thunderbird families.

Intel Pentium 4[3]

Pentium 4 is the 7th generation of Intel x86 family and have a new CPU design, called *NetBurst*, since Pentium Pro was released in 1995. Pentium 4 don´t allow retro-compatibility with other Pentium families, and Intel introduces a new model for power supply units (ATX12), with a dedicated connector for a convenient energy supply of processor. The *Netburst* architecture has 4 new important improvements:

- Hyper Pipelined Technology (from 20 to 31 pipeline stages instead 10 of Pentium III);
- Rapid Execution Engine: this engine have 5 unit of integer processement: 2 ALU´s for simple instructions, 2 GLU´s to write/read data and 1 ALU for complex instructions;
- Execution Trace Cache: only 8 kB L1 cache for data and 12 kB for µop´s, faster and with lower latency than Pentium III L1 cache (32 kB);
- FSB at 400 MHz.

This new design introduces also new 144 faster SSE 2 instructions, a L2 cache with 256 kB and a 64 bit floating point. “Willamette” was the first Pentium 4 and have a 400 MT/s [(2)] front

[1] *Dual Independet Bus*: independent access to memory or L2 cache.

side bus (FSB), which was almost the speed of AMD processors, that have at this time 266 MT/s [(2)], with 256 kB L2 cache ATC on chip.

In 2002, Intel releases the new core of Pentium 4, named Northwood featuring:

- Smaller core (0,13 µm), working at lower voltage and less energy consumption;
- L2 cache with 512 kB ATC on chip;
- FSB at 533 MHz or 800 MHz;
- Hyper Threading[4] consists in a division technology of processor in two logic units (not physical), allowing the execution of 2 instructions in the same clock cycle. 30% faster than Willamette, according with Intel information.
- L3 cache with 2 MB (only in *Extreme Edition*) [5].

The Northwood processor was the first processor working above 3 GHz frequency. Prescott was the last version of this processor family, released on February 2002. Some technicals specifications of Pentium 4 family are below:

Intel Codename	CPU Frequency	FSB/Bandwidth	Cache	Other specifications
Willamette	1.3 GHz - 2.0 GHz	400 mhz/ 3.2 GB/s	8 KB L1 data + 12 KB L1 instruction / 256 KB L2	20 stages pipeline, MMX / SSE / SSE2
Northwood	1.6 GHz - 2.6 GHz	400 MHz / 3.2 GB/s	8 KB L1 data + 12 KB L1 instruction / 512 KB L2	Improved branch prediction and other microcodes tweaks; carried over into subsequent revisions, 21 stages pipeline, MMX / SSE / SSE2
Northwood	2.0 GHz - 3.06 GHz	533 MHz / 4.2 GB/s	8 KB L1 data + 12 KB L1 instruction / 512 KB L2	Improved FSB, hyperthreading only on 3.06 GHz, 21 stages pipeline, MMX / SSE / SSE2
Prescott	From 2.8 GHz up to 3.6 GHz	From 533 MHz / 4.2 GB/s up to 800 MHz / 6.4 GB/s	8 KB L1 data + 12 KB L1 instruction / 512 KB L2 / 2 MB L3	Hypertrheading, addition of on-die L3 cache, from 21 up to 31 stages pipeline, MMX / SSE / SSE2

Table 2 – Generic specifications of Pentium 4 processor

Pentium 4 processors don´t allow multiple processors on the same board. Pentium 4 competes with AMD Athlon, Athlon Thunderbird and Ahtlon XP.

[(2)] **MT** means “megatransfer”. This is a term used to refer a number of data transfers (or operations). It measures the number of transfers per second (MT/s or MT/sec). This mean that 1 MT/s is equal to one million transfers per second.

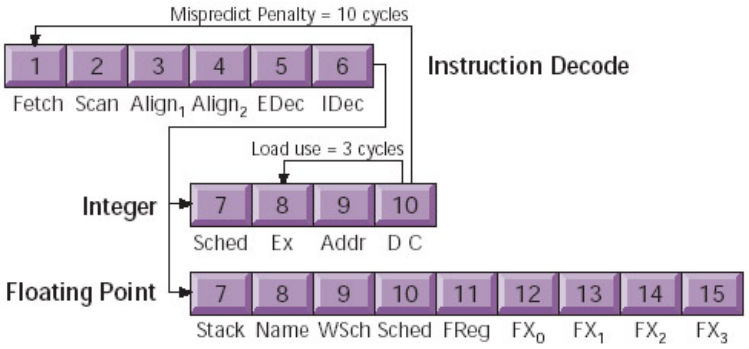
AMD[6]

In April 1997, AMD released K6-III processor (codename *Sharptooth*). This processor have a superscalar micro-architecture, with a RISC core and a CISC decoder, 6 instructions per cycle and . This processor also includes 21 new 3DNow! Instructions[7] (similar to MMX instructions), 64 kB L1 cache and 256 kB L2 cache unit full-speed, both on processor core, and a L3 cache up to 2 Mb, on board.

But after Intel releases Pentium III, AMD K6-III wasn´t faster and after this, AMD releases a new processor family: Athlon (K7 family) [8]. AMD K7 processor was a superscalar x86 micropocessor, with 3 units for integer execution, 3 units of FP and 3 units of calculation addresses. Integer execution pipeline has 10 stages and FP unit have 15 stages.

General improvements of Athlon processors were:

- 24 new *3DNow!* Instructions which allow compatibility with Intel SSE instructions;
- A new floating point unit (3 FP units against 2 FP units in K6-III);
- New bus system, named “Alpha EV-6 Bus”, up to 200 MHz;
- 128 kB L1 cache on chip (full-speed);
- 512 kB or 1 Mb L2 cache off chip (half-speed);
- New prediction system, (*Advanced Dynamic Branch Prediction*);
- Symmetric independent multi processing: allows up to 4 processors working together in the same machine.
- SDRAM with a system bus of 200MHz.



Ilustration 1 – Pipeline structure of K7 processors family [8] (adapted)

The next processor was Athlon Thunderbird, released in June 2000, having 256 kB L2 cache on chip, full-speed, and an EV-6 bus at 266 MHz.

In October 2001, AMD releases Athlon XP Palomino[9] (“e**X**tra **P**erformance”). Morgan (cheaper line) and Palomino core have similar arquitectures, but Palomino needs less 7% energy and was faster, due to SSE instructions compatibility but the new was the multiprocessing. Those processors were also known as Athlon MP (Multprocessing). Palomino was later re-named as Athlon XP Palomino. It features:

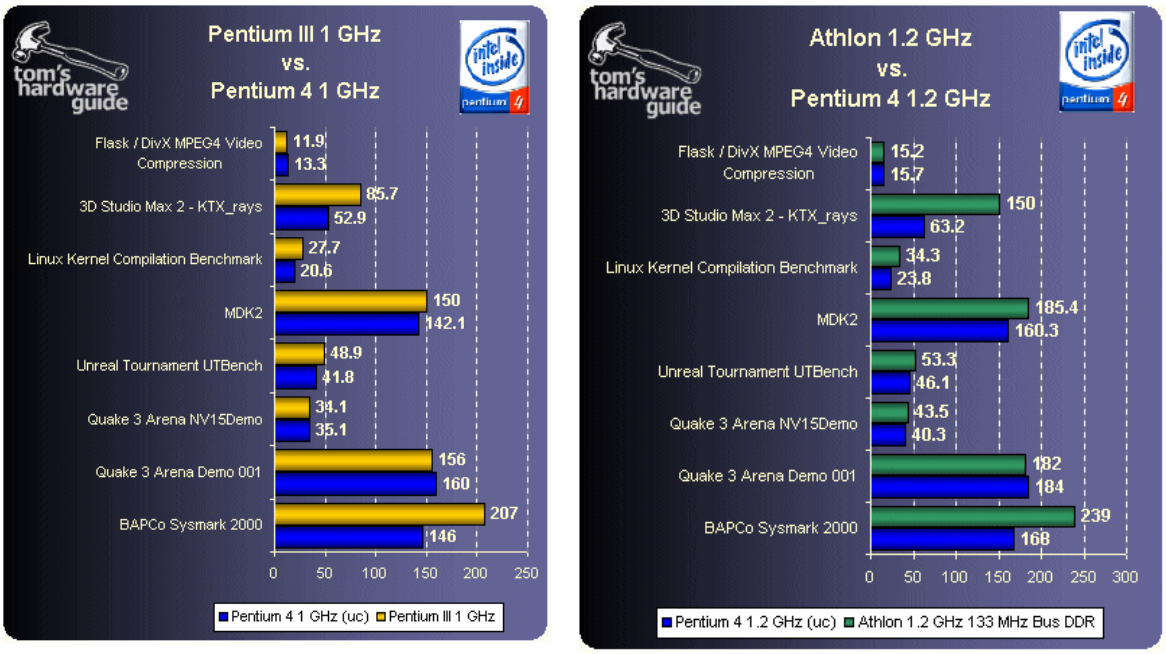
- New 52 new *3DNow!* instructions- named *3D Now! Professional* ;
- New technology *Hardware Data Prefetch*;**[10]**
- *Exclusive and Predictive Translation Lookaside Buffers*;[10]
- Uses *Performance Rating* [11] , comparing its performance with Intel processors performance.

AMD Athlon XP Barton was the last processor from Athlon family. This uses a smaller core, working at lower voltage and produces less heat. Also have a FSB at 333 MHz and 400 MHz, and introduces a L2 cache with 512 kB, on chip.

3 Conclusions

The real improvement of Pentium III are the SSE instructions. Katmai´s size was 0,25 µm what means that Intel implemented a 128 bit architecture using the minimum quantity of silicon as possible. This was made by double-cycling the existing 64-bit data paths and merging SIMD-FP multiplier with the scalar FPU in only one unit, what enables concurrent use of either SIMD-FP and MMX or SIMD-FP and IA-FP double precision floating point code instructions[13]. A great improvement specially for 3D animations.

Against what it was expected, Pentium 4 wasn´t faster than it´s predecessor and, sometimes, it have also worst performance than Pentium III and releases more heat. Also AMD Athlon, which works at lower frequency, was faster in some mathematic operations than the new Pentium 4.



Ilustration 2 - Comparison of PIII vs P4 performance and Athlon vs Pentium 4 [12]

Pentium 4 family have 5 integer processor units: 2 ALU´s for simple instructions, 2 GLU´s to read and write data and 1 ALU for complex instructions. This 5 units were supposed to be faster than the Pentium III, but the 20 stages pipeline take more time to execute the first instruction in Pentium 4, and the last ALU unit is the same used in Pentium III, so Pentium 4 can´t do it faster than Pentium III.

The Netburst P4 provides a higher clock frequency which means more micro-ops per second, but the instructions generates more micro-ops on Pentium 4 than on other processors, which means less instructions per clock cycle. Another disadvantage of the high clock frequency is a long pipeline and, if something goes wrong, there is a bigger penalty. The Pentium 4 has longer latencies than Pentium III or AMD processors for many instructions and this makes it inferior for code with long dependence sequences.[14]

Integer performance of the first Athlon processors are slightly better than that of PIII while floating point performances of Athlon have a significant benefit. This is mainly due to the fact that the Athlon has independent floating point addition and multiplication pipelines that can be run in parallel.

The AMD K7 family uses the opposite strategy of a lower clock frequency, with fewer micro-ops per instruction. This strategy gives better performance for CPU-intensive applications.

The SSE instructions were not an exclusive of Pentium III and 4 but AMD add new 52 instructions that allows parcial compatibility with SSE instructions of Pentium III (70 instructions), and even in low number, those differences allows similar processor frequencies. AMDs processors have a great improvement, putting L1 and L2 cache on-chip, while in the Pentium 4, cache L2 is off chip.

With all these improvements, Pentium 4 processors take RISC philosophy even further by caching micro-ops instead instructions. This result is not convincent since it reduces the amount of information on the cache area and the management of this cache don't take less than a CISC decoder. So, the advantages of going back to CISC design are:

A) CISC code gives better utilization of the limited code cache area;
B) Less micro-ops per instruction gives higher bandwidth in the pipeline;
C) Fewer micro-ops per instruction have a lower energy consumption

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