Mestrado em Informática
&
Curso de Especialização em Informática

Extensions to Instruction Sets

Extensions to Instruction Sets

This communication analyses extensions to instruction sets in general purpose processors their evolution and significant innovation.

- Multimedia and **D**igital **S**ignal **P**rocessing requirements (*overview*)
- Feature detection (*to properly identify the adequate extension*)
- Extensions supported by IA32 based processors (*details*)
- Performance evaluation of each technology
- Case Study – tests and results

Multimedia and DSP requirements

Demand for 2D and 3D graphics, video, audio and other multimedia applications (such as games)

- SIMD – Single Instruction Multiple Data (Vector computation)
  Example: 128 bit registers (16 data of 8 bit each time)
- Floating Point instructions
- DSP computation
  Example: multiply accumulators for *FFT*
- Extensions added to the Instruction Sets

Feature detection

The presence of the **CPUID** instruction is indicated by the ID bit 21 in the EFLAGS register. If this bit is writable, the CPUID instruction is supported

```
pushfd                  ; save EFLAGS
pop eax                 ; store EFLAGS in EAX
mov ebx, eax            ; save in EBX for later testing
xor eax, 00200000h      ; toggle bit 21
push eax                ; put to stack
popfd                   ; save changed EAX to EFLAGS
pushfd                  ; push EFLAGS to TOS
pop eax                 ; store EFLAGS in EAX
cmp eax, ebx            ; see if bit 21 has changed
jz NO_CPUID             ; if no change, no CPUID
```

Code to test for extended functions (EAX=8000_0000h)

```
mov eax, 80000000h      ; query for extended functions
CPUID                   ; get extended function limit
cmp eax, 80000000h      ; is 8000_0001h supported?
jbe NO_EXTENDEDMSR      ; if not, extended technology not supported
```

Extensions in IA32 based processors

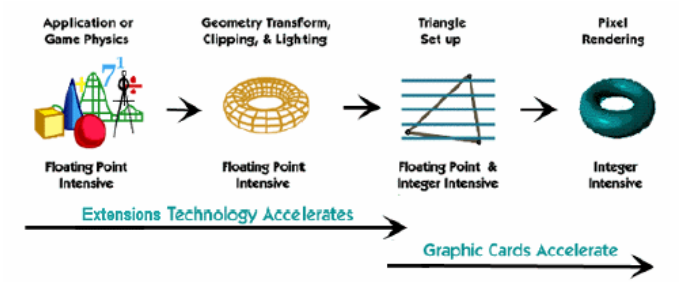
- MMX technology (Intel Architecture)
  - Pentium with new 57 (integer) MMX instructions
- Extended MMX technology (Intel Architecture)
  - Upgrade and extend new instructions on the existing instruction set
- SSE technology (Intel Architecture)
  - Pentium III uses new instructions SSE (MMX2)
  - SSE vs. AMD 3DNow!
  - 71 instructions (52 floating point SIMD instructions, 19 MMX instructions)
- SSE2 technology (Intel Architecture)
  - 144 new instructions when compared with SSE
  - Used in the Pentium 4 processor
  - 128 bit registers, manipulate more data of smaller dimension in each time (for example 16 data of 8 bit each time)
- 3DNow! technology (AMD Architecture)
  - 45 instructions (21 floating point SIMD instructions, 19 new MMX instructions and 5 DSP instructions)

Performance of each technology

Extensions to Instruction Set / CPU map

Processor	MMX	Extended MMX	SSE	SSE2	3DNow!
Intel Pentium					
Intel Pentium MMX	✓				
Intel Pentium II	✓				
Intel Celeron	✓				
Intel Pentium III	✓	✓	✓		
Intel Celeron II	✓	✓	✓		
Intel Pentium 4	✓	✓	✓	✓	
AMD K6	✓				
AMD K6 II - K6 III	✓				✓
AMD Athlon	✓	✓			✓
AMD Duron	✓	✓			✓
AMD Athlon 4	✓	✓	✓		✓

Case Study – tests and results



Graphic Pipeline Functionality

Case Study – tests and results

Compare 2 computers:

- Intel Celeron 800 MHz
- Intel Pentium 4 1.5 GHz

Both have the same graphic card (ATI Radeon), the same monitor and 256 MB RAM

COUNTER-STRIKE

Celeron 800 MHz *Pentium 4 1.5 GHz*