Hardware Requirements for Cellular Processors

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Abstract. Handheld devices require constant adjustments to comply with newer wireless standards and services. Any physical change is a challenge in cost and deadlines. This communication identifies a common architecture backbone for mobile phones and traces a scenario of the hardware requirements for the latest wireless technologies and standards. The architecture of the Intel PXA800F cellular processor is detailed as a case study.

1 Introduction

1.1 Technology Evolution of Mobile Phones

The hardware architecture of mobile phones has suffered several evolutions, which have reduced handsets size, improved communication performance, and minimized power consumption. These evolutions had proper characteristics along spaces of time, which has driven to identify them as generations.

The first generation (1G) of mobile cellular technology saw two key improvements during the 1970s: the evolution of the microprocessor and the digitization of the control link between the mobile phone and the cell site. The greater expansion of this technology was in the early 1980's but with very limited features, poor voice quality, and limited radio coverage. The systems were “cellular” because coverage areas were split into smaller areas or “cells”, each of which is served by a low power transmitter and receiver.

In the end of 80’s / early 90's, the second generation (2G) of mobile phones appeared, based in digital networks, but with a poor quality due to a low bit rate digitization. These systems digitized not only the control link but also the voice signal. Shortly, the new system started to provide better quality and higher capacity at lower cost to consumers. The Global System for Mobile Communications (GSM) was adopted as the standard technology for mobile phones.

The first implementation of third generation (3G) cellular phones was deployed in Japan in 2001. At Europe, for now, it is a promise of faster communications services, including voice, fax and Internet, anytime and anywhere with seamless global roaming. This generation adopts the ITU’s IMT-2000 global standard which enables applications and services like multimedia entertainment, infotainment and location-based services.

Recently, the Enhanced Data Rates for Global Evolution technology (EDGE) emerged. Although it is considered a 3G technology, EDGE enhances the coding of the GSM/GPRS radio interface in existing frequency bands (GSM operators can offer typical user data rates of 100-120kbit/s, with up to 384kbit/s available under good conditions - enough to handle video smoothly). Since EDGE is fully compliant with IMT-2000 3G technology, it is considered the bridge between 2G and 3G, enabling operators to use existing GSM radio bands to offer mobile multimedia IP-based applications at speeds of up to 384kbit/s with a bit-rate of 48kbit/s per time slot.

Actually technologies use an intermediate stage between 2G and 3G, denominated 2.5G. Examples of that kind of technologies are Global Packet Radio Service (GPRS) and Universal Mobile Telecommunications System (UMTS).

1.2 Hardware Backbone

Although each company has its own cellular phone hardware architecture, it is possible to identify a common hardware backbone for all of them. These devices contain at least the following elements: a screen, a keyboard, audio transducers (microphone and loudspeaker), an ICC connector to access the SIM/USIM card and a battery. Other optional elements could be provided, such as specific audio equipment (pedestrian kit) or data interfaces (serial link, IrDA, Bluetooth).

Digital cellular phones are based on a common architecture made up of two major modules (Fig. 1): a "Radio frequency" block which handles the radio aspects and the physical interface with the network; a "Base band" block to manage the high layers of the protocol, the applications and to control the human interface [1].

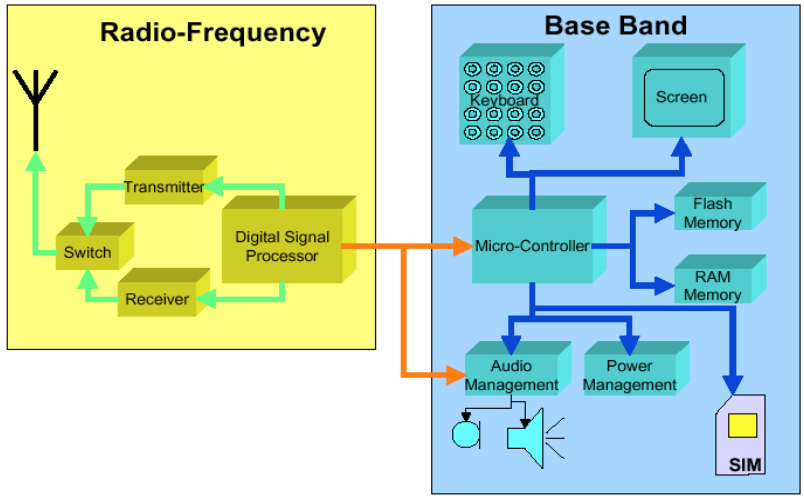

Fig. 1. General Mobile Phones Hardware Architecture (source: CEN [1])

2 Requirements for New Mobile Phones Hardware Architectures

To establish these requirements it is necessary to identify the actual technology and its evolution.

Currently, conversational speech is the main service of mobile phones systems, but the requests to support data communications over-the-air interface is quickly increasing. The evolution of cellular phones technology leads into the General Packet Radio Service (GPRS). This new technology lets information to be sent and received across a mobile telephone network, supplements today's Circuit Switched Data and Short Message Service and, theoretical, supplies maximum speeds of up to 40kbps. GSM operators with additional 2GHz radio spectrum are able to introduce wideband radio access with UMTS, to give user data rates of up to 2Mbit/s. EDGE is the emergent technology, which is basically translated into more information in quantity and diversification.

To support the requirements of these recent and future technologies, the mobile phones hardware has to have some special characteristics:

Evolution Capacity. Today is important that hardware devices as microprocessors have the capacity to stand in market for a sufficient time to make their research became lucrative. With constant evolution of technologies and wireless standards, this only could be achieved with devices able to evolutes/adapts or to be integrated in a newer device that perform the necessary upgrade.
Large Application Field. A hardware component/device has yours value improved as larger was the number of different applications supported and others devices where it could be used. A way to achieve this goal is to integrate capacity to execute as more as possible different tasks in a single chip. However, the multi-functionality of these devices puts some constraints in terms of size, cost and especially energy dissipation.
Higher Bit-Rates. The bit transmission requires an amount of energy per bit. More bit-rates leads to more energy spend. Higher bit-rates also require a linear increase in spectral bandwidth, a sparse resource. In fact, wireless designers are increasingly challenged to jam more bits into a narrower band, or to increase the capacity of their system (in bits/sec/Hz). Doing so requires **extensive signal-processing**, with complex but faster computational resources.
Reduced Power Consumption. The power consumption achieves a large position in wireless devices needs, since is directly relational with the device mobility and battery life-time. One important achieve to reduce consume is the low power standby mode and the deactivation of the system modules when in idle time. The power consume is direct or indirectly associated with all others hardware architecture issues.
Small Area. The size and weight take influence in the handset portability. This is not an insignificant characteristic for wireless devices. In the last decade was observed an increase of computers complexity, improving these machines with powerful processors and multi-tasks, which have been maintaining computer total size considerable. With mobile phones, all technology has to be concentrated in a hand area. So, the technology and functions to be introduced in handheld devices has a limit.
High Processor Performance. Using RISC processors, the handheld devices gains in specific and simple instructions processing, but with the raise of sophistication on applications to make the product interesting to clients, drive to an increase of algorithms/applications complexity and a consequent decrease of processor performance. To attend the wireless demands, new processors are increasing the number of transistors per chip, improving general-purpose CPU and DSP performance, but fundamental bounds are being pushed, as limits on instruction-level parallelism and limits on memory system performance. New architectures realize only 2-3 instructions/clock and there is a progressive cache's enlargement to hide DRAM latency [2], [3], [4], [5].

3 Ideal Cellular Processor Model

Assembling all the requirements, a model for today's cellular phones hardware architecture is achieved, which is a kind of all-in-one. It has to be heterogeneous, support massive concurrency, match the computational model, operate at minimum supply voltage and clock frequency, and provide flexibility only where needed and desirable and at the right granularity. In resume, it combines performance, flexibility and energy-efficiency (Fig.2) [5].

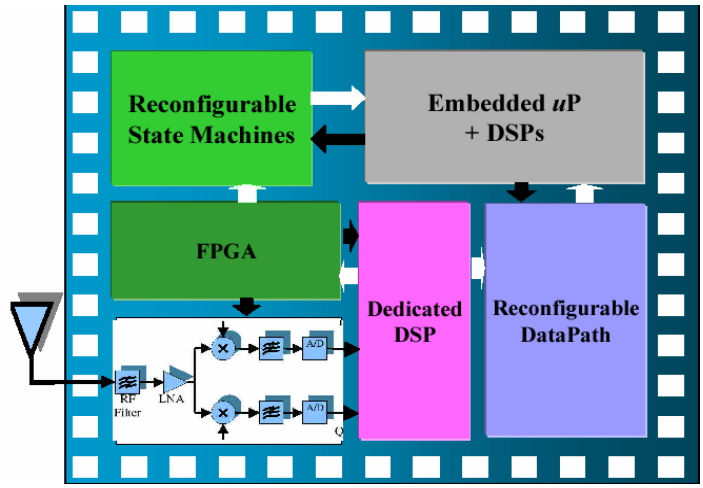

Fig.2. The ideal "all-on-one" architecture (courtesy of Jan M. Rabaey)

3.1 Signal Acquisition

The information arrives at a cellular phone through the antenna. That analog information is then conditioned (filters, amplifiers …) and converted to a digital signal, passive of be understand by DSP module. This section is often placed outside of cellular processors because of their considerable noise inherent to analog circuits with high frequency signals.

3.2 FPGA

A Field-Programmable Gate Array is a hardware matrix of cells where the logic network can be programmed into the device after its manufacture. The cells are logic elements such as gates, lookup table RAMs, flip-flops and programmable interconnect wiring. With these properties, FPGAs becomes a fast and relatively inexpensive realization of specialized programmable cellular processors for arbitrary operations. Moreover, the same FPGA hardware could be reused several times, with different specialized applications.

3.3 Reconfigurable State Machines

A state machine is formal defined by the five-tuple M= {I, S,Z, δ, λ} where: I is the input set; S is the state set; Z is the output set; δ=SxI→S is the state transition function; λ=SxI→Z is the output function. A reconfigurable state machine is capable to change the the tuple elements characteristics, either by self induction or by external factors. Such machine provides flexible digital control over other cellular processor modules, optimizing de automatic state change of the system, in response to a new condition or information received (ex: standby) [6].

3.4 Reconfigurable DataPath

The DataPath is where arithmetic computations take place, i.e., the HW from the data input bus to the data output bus. An ideal cellular processor should have a short and efficient DataPath. This characteristic interfere on time spend in memory access. Their correct management leads to an increase of processing speed. With a reconfigurable DataPath, a cellular processor could adapt the path of distinct data, matching the possible system alterations in real-time. For example if a congestion occurs at a determinate bus, the data could be send by another bus (if exists), saving their dependent processes to crash.

3.5 Embedded Microprocessor and DSPs

A general purpose microprocessor handles the aplication level, processing all the information and services that perform the interface Man-Machine. It should be an embedded microprocessor running at absolute minimal rates (power consume, clock frequency) with high processing capacity. A Digital Signal Processor (DSP) provides the processor with an extended set of instructions for digital signal processing. The µP+DSPs design methodology may lead to a software organization that decides which parts of the application will be performed in each processor. The advantage is to have a multifunction core in a smaller area, with faster communication between both.

3.6 Dedicated DSP

Digital Signal Processors receives digitized signals like voice, audio, video, temperature, pressure, or position and then mathematically manipulate them. This manipulation requires a DSP design oriented to achieve high performance in execution of mathematical functions like add, subtract, multiply and divide. Since cellular phones receives a large amount of complex information by Radio Frequency (RF) its necessary a powerful DSP to process this information. In an ideal cellular processor is expected that a DSP performs repetitive numeric computations. Since the multiply operation is the most complex operation, it needs a fast MAC (Multiplication and accumulation) unit. Some cellular processors use multi-MAC architecture, with parallel multiply-accumulate units that greatly improve de signal process performance (Fig.3). Other bottleneck of DSP performance is memory access. To resolve that could be used a multi-bus structure that performs multiple memory access and specialised addressing modes to achieve instructions/data more efficiently. Other approach is a memory on chip architecture that reduces the datapath improving processing speed. A DSP have to have also real-time processing capability and low power dissipation. These characteristics justify a dedicated core. If the processor doesn't spend resources in other general actions, save performance to their DSP specific functions [7].

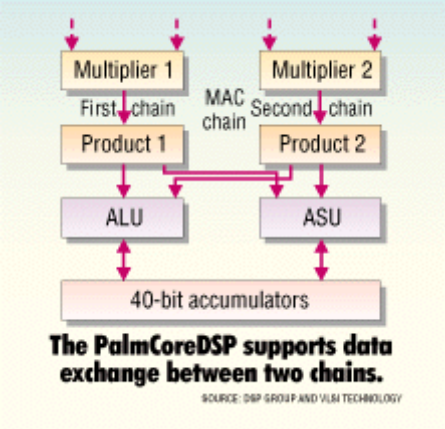

Fig.3. Multi-MAC DSP architecture

4 Examples of cellular processors

To illustrate what is being developed recently in mobile phones processors, it's now indicated some of those technologies and a few examples of them announced characteristics.

Philips' Nexperia. This mobile video/multimedia processor, recommended for smartphones handsets, will be available on the open market from early 2004. This processor is currently used in the P800 Smartphone of Sony Ericsson Mobile Communications. The mobile multimedia processor combines System on Chip design and media processing and connectivity.
Motorola's i.MX Processors Family. Embedded application processors based on ARM technology, offers a leap in performance and integration from earlier DragonBall™ processor products. Motorola bet in performance and stamina and announces that next generations of the i.MX family will incorporate advanced floating-point technology in hardware.
Texas Instruments's OMAP1710. Expected to sample in the first quarter of 2004, the OMAP1710 device offers up to 40 percent improvement in performance for a variety of mobile applications, while consuming as little as half the power of current TI application processors. Provide mix of multimedia features and cost-effectiveness, making them more attractive to the high-volume market for multimedia smartphones. Include an ARM processor and a TI DSP engine and supports advanced mobile operating systems such as Linux, Microsoft´s Windows Mobile, Nucleus, Palm OS and Symbian OS.

Because of their approach to the ideal mobile phone processor architecture shown above, it's considerate the Intel PXA800F processor as a specific solution case study.

5 PXA800F Cellular Processor

The Intel PXA800F Cellular Processor is a fully integrated DSP and application cellular processor for today's GSM/GPRS mobile phones (Fig.4).

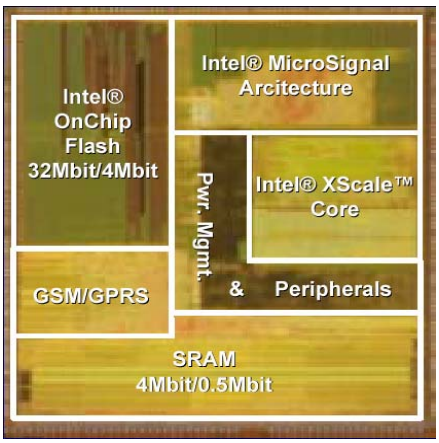

Fig.4. Intel PXA800F cellular processor architecture (courtesy of Dilip Krishnaswamy, Intel Corporation)

The plan in this processor is to incorporate a maximum number of functionalities in one single chip, betting in adaptable hardware instead of reconfigurable hardware. The main blocks of the PXA800F are Micro Signal Architecture (MSA) and XScale technologies, each of this ones function as an independent processor. This capability is provided by having each a dedicate instruction and data cache, Flash and SRAM.

The XScale is an application processor, with a maximum frequency of 312MHz. However, it is capable to adjust over a wide range of speed and power consume, according with the needs of the application, increasing the system performance. This core process all the information associated with the GSM/GPRS protocol stack. To increase the independence level, this block have microcontroller capacities, that allows the integration

with peripherals such as an LCD controller, multi-media controllers, external memory interface or a network processor [9].

The MSA is a DSP processor with a maximum frequency of 104MHz. It has the DSP capacities mentioned in section 3.6 and also special instructions to maximize performance for GSP/GPRS, including Viterbi and digital signal filtering instructions. The module independence is provided, as already mentioned, by a dedicate memory sub-system and also by microcontroller capacities. In opposition of the XScale peripherals, suited for use with application related functions, the MSA peripherals are RF related [8].

5.1 Where PXA800F Converge With Ideal Cellular Processor Model

Two perfectly distinct blocks were established in section 1.2 in cellular phones hardware architecture (Radio Frequency and Base Band). In Fig. 5 it is possible to distinguish clearly these two blocks and how PXA800F different modules interact with those. From the backbone Radio Frequency block, the Intel processor features the Digital Signal Processor, and adds dedicated memory system and controller functions (right side on figure). From the Base Band, it features the Micro-Controller capacities, Flash and RAM memories (left side on figure). The other components in the figure are peripherals.

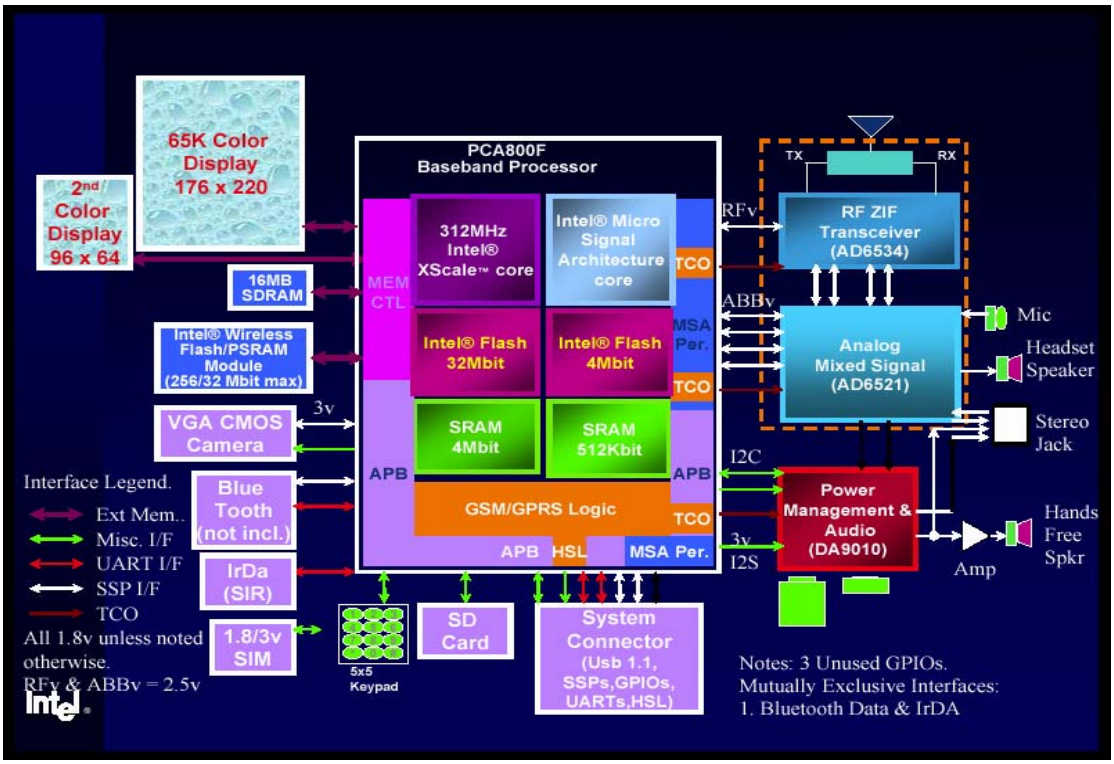

Fig. 5. The PXA800F integration (courtesy of Dilip Krishnaswamy, Intel Corporation)

From the ideal cellular processor model, PXA800F adopts the dedicated DSP, improving this section with microcontroller capacities (MSA), and the embedded µP (XScale). The FPGA and reconfigurable state machines model was declined, preferring a multi-function adaptive and scalable approach. The hardware does not change, but it allows functionality during a sufficient in-market lifetime.The reconfigurable datapath was also declined, opting for a separation of applications data and specific DSP data. Because XScale an MSA does not have to share memory-subsystems, the data has specific paths, according with data type. However, multi-buses provide alternative corridors for data [10].

6 Conclusions

By performing the integration of MSA and XScale on a single chip, the PXA800F gains in size reduction and larger application field. The integration of dedicated memory-systems decreases the power consumption and the time spent to access external memory. The multifunctional processor also allows integration with several types of peripherals and the capacity to evolve to new stages, just by software upgrading (PXA800EF).

Although the Intel cellular processor PXA800F does not exactly follow the ideal model presented above, it has the essential requirements mentioned in section 2, which may be considered adjusted for today's cellular technology challenges.

It is difficult to determine where the limit to the mobile phones architecture evolution is. The industries are betting on more transistors in a same or smaller area, with multi-function/programmable hardware and scalability. These methods have some risks, for example the nightmare in what could become a super processor with uncountable functions and great speed that is used to perform only one simple task not time critical. This is a waste of capacity that had the respective cost effects. And when it is necessary to perform a new function that the processor can not handle? The solution may be to keep some specific devices simpler, but more efficient and cheaper to replace. On the other hand, it could be achieved a stage of integration technology so efficient that the overall system becomes a “bargain”. This stage is possibly the introduction of biologic gates to replace transistors, but for now is just a futurist vision.

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